THAT WHICH IS CLAIMED:

1. A scalable computer architecture capable of performing fully scalable simulations, said architecture comprising:

a plurality of processing elements; and

a plurality of interconnections between the plurality of processing elements capable of interconnecting the plurality of processing elements, wherein at least two interconnections interconnect each processing element to at least two other processing elements, wherein at least one interconnection further interconnects at least one processing element to at least one other processing element located remote from the respective at least one processing element,

wherein the computer architecture supports variations in the number of processing elements, and wherein the number of interconnections between processing elements is independent of the number of processing elements so that the number of processing elements is capable of changing without similarly changing the number of interconnections between processing elements, thereby permitting connectivity between the processing elements to be scalable.

2. A scalable computer architecture according to Claim 1, wherein the plurality of interconnections interconnect the plurality of processing elements according to a fractal-type method.

3. A scalable computer architecture according to Claim 1, wherein the plurality of interconnections interconnect the plurality of processing elements according to a quenched random method.

4. A scalable computer architecture according to Claim 1, wherein the plurality of interconnections include at least one interconnection at each length scale of the plurality of processing elements.

5. A scalable computer architecture according to Claim 1, wherein the plurality of processing elements are organized in a one-dimensional topology.

6. A scalable computer architecture according to Claim 1, wherein the plurality of interconnections connect each processing element to each neighboring processing element located adjacent the respective processing element, and wherein at least one interconnection further connects at least one processing element to at least one other processing element located remote from the respective at least one processing element.

7. A scalable computer architecture according to Claim 1, wherein the plurality of processing elements are organized in a multi-dimensional topology, wherein the dimension of the multi-dimensional topology is greater than one.

8. A scalable system to facilitate fully scalable simulations comprising a plurality of processing elements, wherein each processing element capable of being interconnected to at least two other processing elements, wherein at least one processing element is further capable of being interconnected to at least one other processing element located remote from the respective at least one processing element, wherein the scalable system supports variations in the number of processing elements, and wherein the number of other processing elements interconnected to each processing element is independent of the number of processing elements so that the number of processing elements is capable of changing without similarly changing the number of other processing elements interconnected to each processing element, thereby permitting connectivity between the processing elements to be scalable.

9. A scalable system according to Claim 8, wherein the plurality of processing elements are interconnected according to a fractal-type method.

10. A scalable system according to Claim 8, wherein the plurality of processing elements are interconnected according to a quenched random method.

11. A scalable system according to Claim 8, wherein the plurality of processing elements are interconnected such that at least one pair of processing elements are interconnected at each length scale of the plurality of processing elements.

12. A scalable system according to Claim 8, wherein the plurality of processing elements are organized in a one-dimensional topology.

13. A scalable system according to Claim 8, wherein the plurality of processing elements are organized in a multi-dimensional topology, wherein the dimension of the multi-dimensional topology is greater than one.

14. A scalable system according to Claim 8, wherein the each processing element is interconnected to each neighboring processing element located adjacent the respective processing element, and wherein at least one processing element is interconnected to at least one other processing element located remote from the respective at least one processing element.

15. A method of fabricating a scalable computer architecture capable of performing fully scalable parallel discrete event simulations, said method comprising:

organizing a first number of processing elements; and

interconnecting the first number of processing elements so that each processing element is interconnected to at least two other processing elements, and so that at least one processing element is further interconnected to at least one other processing element located remote from the respective at least one processing element,

wherein the number of other processing elements interconnected to each processing element is independent of the number of processing elements so that the number of processing elements is capable of changing without similarly changing the number of other processing elements interconnected to each processing element, thereby permitting connectivity between the processing elements to be scalable.

16. A method according to Claim 15, wherein interconnecting the plurality of processing elements comprises interconnecting the plurality of processing elements according to a fractal-type method.

17. A method according to Claim 15, wherein interconnecting the plurality of processing elements comprises interconnecting the plurality of processing elements according to a quenched random method.

18. A method according to Claim 15, wherein interconnecting the plurality of processing elements comprises interconnecting the plurality of processing elements such that at least one pair of processing elements are interconnected at each length scale of the plurality of processing elements.

19. A method according to Claim 15, wherein organizing the plurality of processing elements comprises organizing the plurality of processing elements in a one-dimensional topology.

20. A method according to Claim 15, wherein organizing the plurality of processing elements comprises organizing the plurality of processing elements in a multi-dimensional topology, wherein the dimension of the multi-dimensional topology is greater than one.

21. A method according to Claim 15, wherein interconnecting the plurality of processing elements comprises interconnecting the each processing element to each neighboring processing element located adjacent the respective processing element, wherein at least one processing element is interconnected at least one other processing element located remote from the respective at least one processing element.

22. A method according to Claim 15 further comprising:

changing the number of processing elements to a second number; and

interconnecting the second number of processing elements so that each processing element is interconnected to at least two other processing elements, and so that at least one processing element is further interconnected to at least one other processing element located remote from the respective at least one processing element,

wherein the number of other processing elements interconnected to each processing element is independent of the number of processing elements so that the number of processing elements is capable of changing from the first number to the second number without similarly changing the number of other processing elements interconnected to each processing element, thereby permitting connectivity between the processing elements to be scalable.